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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,600	09/16/2005	Uwe Guenther	10191/4126	9491

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EXAMINER	
WILLIAMS, HOWARD L	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,600	GUENTHER ET AL.	
	Examiner	Art Unit	
	Howard L. Williams	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 10, 13, 15, and 16 are rejected under 35 U.S.C. 102(b) as anticipated by Hasegawa (US 5203945 A). Hasegawa discloses a system for serial data transmission from a first station (parallel-serial 20; fig. 1) to a second station (serial-parallel, 30; fig. 1). The first station includes a first shift register (22: fig. 1). The second station includes a second shift register (32; fig. 1). The clock unit corresponds to the timing control box (60) and furnishes a clock signal directly connected to both the first and second stations/shift registers automatically clocking the shift registers. In column two Hasegawa discloses that the arrangement reduces the load on the control means/CPU.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. (US 20010044862 A1). Mergard discloses a method for serially transmitting data between a first station (406; fig. 4) and second station (418; fig. 4). Mergard provides the serial transmission to free up pins (para 0008). The serial-to-parallel converters and parallel-to-serial converters are labeled simply converters in figure 4 (202D, 202F) but are shown with a parallel input and serial output for 202D so it receives at least two signals and serially transmits these signals to the second station (418). Mergard does not disclose the serial-to-parallel converter and parallel-to-serial converter as shift registers. However, shift registers are well known for that purpose

and the use of shift registers configured to provide parallel-to-serial conversion and vice-versa would have been obvious to one of ordinary skill in the art.

Mergard discloses a system with embedded controllers. In figure 1 the processor is element 100 and figure 2 discloses the bus controller and additionally includes a serial bus controller. Mergard thus appears to not load the processor 100. The controllers 202A, 202B, and 202C intercede between the embedded controller processors.

The response points out a number of signals furnished by the processor to the bus controller and serial bus controller, arguing that the processor is clearly loaded. These citations are not seen to support the point urged. These signals are furnished to the bus controller thereby absolving the processor of having to manage the serial transmission directly. Contrasted with applicants figures which do not show where the data to be serially transmitted comes from -- the serial transmission does not just pull it out of thin air-- something in applicants' circuit is loaded to supply the data to the "first station.

Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada (JP 11-178349 A). Shimada discloses two stations with serial transmission between them to reduce the to reduce the number of transmission lines for transferring the gate signals. The clock circuit is 13. The serial-to-parallel and parallel-to-serial converters are 14 and 12. Yamada does not discuss the clock rate in the abstract but it would have been obvious to select a clock of sufficient speed such that bits would not be missed. Yamada also does not disclose the serial-to-parallel and parallel-to-serial converters as shift registers however it is considered that it would have been obvious to one of ordinary skill that shift registers are commonly used for this purpose.

A machine translation (attached) of Shimada's desription of the drawings reveals the clock as 13 rather than 11 and the S-P and P-S elements as shift registers.

Claims 9-11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US 5475831 A). Yoshida discloses a serial transmission system that includes a shift register for the serialization/deserialization function and is driven by the clocking circuitry. It is fed from the buffer which provides isolation between the CPU and the serializer such that the CPU does not need to directly control the serialization. The Yoshida discloses that this arrangement reduces the load on the CPU (col.4 line 1) so it would have been obvious that the serializer transmits without loading the CPU.

Applicants' response filed 23 February 2007 has been fully considered but it is not persuasive. The instant claims recite a method of transmitting data serially and include the shift registers and clock. Applicants simply are not the first persons to conceive of serial data transmission.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office central facsimile number for application specific correspondence intended for entry is 571-273-8300.

5/2/07
Voice: (571) 272-1815

Howard L. Williams
Primary Examiner
Art Unit 2819